

REMARKS

Claims 1-3, 6-19, and 22-40 were examined and reported in the Office Action. Claims 1-3, 6-19, and 22-40 are rejected. Claims 1, 10, 17, 24, 29 and 36 are amended. Claims 1-3, 6-19, and 22-40 remain.

Applicant requests reconsideration of the application in view of the following remarks.

I. 35 U.S.C. § 102

It is asserted in the Office Action that claims 10, 12-14, 24 and 26 are rejected under 35 U.S.C. § 102(b), as being anticipated by *Simulation based architectural power estimation for PLA-based Controllers*, August 1996, Low Power Electronics and Design, 1996, International Symposium on, 12-14, Pages: 121-124, Katkoori et al. ("Katkoori"). Applicant respectfully disagrees.

According to MPEP §2131, "[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' (Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)). 'The identical invention must be shown in as complete detail as is contained in the ... claim.' (Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989)). The elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, *i.e.*, identity of terminology is not required. (In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990))."

Applicant's amended claim 10 contains the limitations of "...determining an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA; dividing the set of equations representing the PLA into equations representing the plurality of sub-PLAs ; merging outputs of the equations representing the plurality of

sub-PLAs; determining a topological circuit representation of the equations representing the plurality of sub-PLAs; applying gating logic to the topological circuit representation of the plurality of sub-PLAs; and controlling power consumption in the topological representation of the plurality of sub-PLAs so only one of the plurality of sub-PLAs contributes to power consumption, wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA."

Applicant's amended claim 17 contains the limitations of "...determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each have an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA; divide the set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable; determine a topological circuit representation of first sub-PLA and the second sub-PLA; apply gating logic to the topological circuit representation of the first sub-PLA and the second sub-PLA; and control power consumption in the topological circuit representation of the first sub-PLA and the second sub-PLA so only one of the first sub-PLA and the second sub-PLA contributes to power consumption, wherein the topological circuit representation an OR plane of the first sub-PLA is interleaved with an OR plane of the second sub-PLA."

Applicant's amended claim 24 contains the limitations of "...determine an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA; divide the set of equations representing the PLA into equations representing the plurality of sub-PLAs; merge outputs of the equations representing the plurality of sub-PLAs; determine a topological circuit representation of the equations representing the plurality of sub-PLAs; apply gating logic to the topological circuit representation of the plurality of sub-PLAs; and control power consumption in the topological circuit

representation of the plurality of sub-PLAs so only one of the plurality of sub-PLAs contributes to power consumption, wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA.”

It is asserted in the Office Action that Katkoori discloses a plurality of sub-PLAs. Figure 1 of Katkoori only illustrates a PLA (i.e., not a sub-PLA) shown in an exploded AND-OR structure. If, however, Katkoori’s illustrated PLA is sub-components (i.e., sub-PLAs), Katkoori does not teach, disclose or suggest that each sub-PLA component (i.e., each sub-PLA) has an OR plane. This is quite clear as the illustrated AND plane, input buffers and output buffers do not teach, disclose or suggest to include an OR plane. In other words, Applicant’s sub-PLAs are each PLAs broken out from the original PLA (i.e., sub-PLAs).

Katkoori discloses a scheme for power simulation of a PLA. To simulate the power consumption of a PLA, Katkoori discloses that first a PLA is synthesized by varying equations to achieve the desired ranges that would result in the average capacitance switched by a node. Next, an input vector sequence is used to switch nodes, and then values are extracted. The values that were extracted are then used to derive a set of equations by using curve fit algorithms, resulting in node switching capacitance (NSC) equations. These equations are then used in a power estimator. Nowhere does Katkoori disclose, teach or suggest “determining an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA” or “determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each have an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA.”

Therefore, since Katkoori does not disclose, teach or suggest all of Applicant’s amended claims 10, 12 and 24 limitations, Applicant respectfully asserts that a *prima*

facie rejection under 35 U.S.C. § 102(b) has not been adequately set forth relative to Katkoori. Thus, Applicant's amended claims 10, 12 and 24 are not anticipated by katkoori. Additionally, the claims that directly or indirectly depend on claims 12 and 24, namely claims 13-14, and 26, respectively, are also not anticipated by Katkoori for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 102(b) rejections for claims 10, 12-14, 24 and 26 are respectfully requested.

II. 35 U.S.C. § 103

A. It is asserted in the Office Action that Claims 1-3, 6-9, 17-19, 22-23 and 29-40 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over U. S. Patent No. 5,311,079 issued to Ditlow in view of U.S. Patent Application No. 6,492,835 issued to Shau ("Shau"). Applicant respectfully disagrees.

According to MPEP §2142 "[t]o establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." (In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)). Further, according to MPEP §2143.03, "[t]o establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974)." "*All words in a claim must be considered* in judging the patentability of that claim against the prior art." (In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970), emphasis added.)

Applicant's amended claim 1 contains the limitations of "...determining an optimum splitting variable for dividing a programmable logic array (PLA) into a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane,

said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA; dividing a set of equations representing a PLA into a first set of equations representing a first sub-PLA and a second set of equations representing a second sub-PLA based on the splitting variable; determining a topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; and controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption, wherein an OR plane of the topological circuit representation of the first sub-PLA is interleaved with an OR plane of the topological circuit representation of the second sub-PLA."

Applicant's amended claim 17 contains the limitations of "...determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each have an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA; divide the set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable; determine a topological circuit representation of first sub-PLA and the second sub-PLA; apply gating logic to the topological circuit representation of the first sub-PLA and the second sub-PLA; and control power consumption in the topological circuit representation of the first sub-PLA and the second sub-PLA so only one of the first sub-PLA and the second sub-PLA contributes to power consumption, wherein the topological circuit representation an OR plane of the first sub-PLA is interleaved with an OR plane of the second sub-PLA."

Applicant's amended claim 29 contains the limitations of "...determining an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each

having an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA; dividing the set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable; determining a topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; applying gating logic to the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA; and controlling power consumption in the topological circuit representation of the equations representing the first sub-PLA and the equations representing the second sub-PLA so only one of the topological circuit representation of the first sub-PLA and the second sub-PLA contributes to power consumption, wherein an OR plane of the topological circuit representation of the first sub-PLA is separated from an OR plane of the topological circuit representation of the second sub-PLA."

Applicant's amended claim 36 contains the limitations of "...determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each having an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA; divide a set of equations representing the PLA into a first set of equations representing the first sub-PLA and a second set of equations representing the second sub-PLA based on the splitting variable; determine a topological circuit representation of the first sub-PLA and the second sub-PLA; apply gating logic to the topological circuit representation of the first sub-PLA and the second sub-PLA; and control power consumption in the topological circuit representation of the first sub-PLA and the second sub-PLA so only one of the first sub-PLA and the second sub-PLA contributes to power consumption, wherein in the topological circuit representation an OR plane of the first sub-PLA is separated from an OR plane of the second sub-PLA."

Ditlow discloses a PLA having a decoder attached at the input of the PLA to only power up a portion of the PLA to minimize power consumption. Ditlow does not teach, disclose or suggest dividing a PLA into sub-PLAs where each sub-PLA has an OR

plane. That is, Ditlow does not teach, disclose or suggest “determining an optimum splitting variable for dividing a programmable logic array (PLA) into a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA,” “determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each have an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA,” “determining an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each having an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA,” or “determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each having an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA.”

Shau discloses power saving methods for PLAs including splitting a PLA into sub-PLAs based on minterms. (Shau, column 7, line 15 to column 8, line 47). Shau, however, does not determine an optimum splitting variable for dividing a PLA into a plurality of sub-PLAs, where the splitting variable corresponds to a specific input, output and product in a set of equations representing the PLA.

Therefore, even if Ditlow were combined with Shau, the resulting invention would still not include all of Applicant’s claimed limitations. And, therefore, there would be no motivation to combine Ditlow with Shau.

Moreover, by viewing the disclosures of Ditlow and Shau, one can not jump to the conclusion of obviousness without impermissible hindsight

According to MPEP 2142, [t]o reach a proper determination under 35 U.S.C. 103, the examiner must step backward in time and into the shoes worn by the hypothetical ‘person of ordinary skill in the art’ when the invention was unknown and just before it

was made. In view of all factual information, the examiner must then make a determination whether the claimed invention 'as a whole' would have been obvious at that time to that person. Knowledge of applicant's disclosure must be put aside in reaching this determination, yet kept in mind in order to determine the 'differences,' conduct the search and evaluate the 'subject matter as a whole' of the invention. The tendency to resort to 'hindsight' based upon applicant's disclosure is often difficult to avoid due to the very nature of the examination process. However, impermissible hindsight must be avoided and the legal conclusion must be reached on the basis of the facts gleaned from the prior art." Applicant submits that without first reviewing Applicant's disclosure, no thought, whatsoever, would have been made to splitting a PLA into sub-PLAs by use of an optimum splitting variable and gating so only one of the sub-PLAs contributes to power consumption.

Neither Ditlow, Shau, nor the combination of the two, teach, disclose or suggest the limitations contained in Applicant's amended claims 1, 17, 29 and 36, as listed above. Since neither Ditlow, Shau, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claims 1, 17, 29 and 36, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claims 1, 17, 29 and 36 are not obvious over Ditlow in view of Shau since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 1, 17, 29 and 36, namely claims 2-3 and 6-9, 18-19, 22 and 23, 30-35, and 37-40, respectively, would also not be obvious over Ditlow in view of Shau for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 1-3, 6-9, 17-19, 22-23, and 29-40 are respectfully requested.

B. It is asserted in the Office Action that Claims 11 and 25 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Katkoori in view of Shau. Applicant respectfully disagrees.

Applicant's claim 11 depends on amended claim 10. Applicant's claim 25 depends on Applicant's amended claim 24.

Applicant's amended claim 10 contains the limitations of "...determining an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA; dividing the set of equations representing the PLA into equations representing the plurality of sub-PLAs ; merging outputs of the equations representing the plurality of sub-PLAs; determining a topological circuit representation of the equations representing the plurality of sub-PLAs; applying gating logic to the topological circuit representation of the plurality of sub-PLAs; and controlling power consumption in the topological representation of the plurality of sub-PLAs so only one of the plurality of sub-PLAs contributes to power consumption, wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA."

Applicant's amended claim 24 contains the limitations of "...determine an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA; divide the set of equations representing the PLA into equations representing the plurality of sub-PLAs ; merge outputs of the equations representing the plurality of sub-PLAs; determine a topological circuit representation of the equations representing the plurality of sub-PLAs; apply gating logic to the topological circuit representation of the plurality of sub-PLAs; and control power consumption in the topological circuit representation of the plurality of sub-PLAs so only one of the plurality of sub-PLAs contributes to power consumption, wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA."

Katkoori is discussed above in section I regarding Applicant's amended claims 10 and 24. As asserted above, Nowhere does Katkoori disclose, teach or suggest "determining an optimum splitting variable for dividing a set of equations representing

a programmable logic array (PLA) into equations representing a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA” or “determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each have an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA.”

Shau discloses power saving methods for PLAs including splitting a PLA into sub-PLAs based on minterms. (Shau, column 7, line 15 to column 8, line 47). Shau, however, does not determine an optimum splitting variable for dividing a PLA into a plurality of sub-PLAs, where the splitting variable corresponds to a specific input, output and product in a set of equations representing the PLA.

Moreover, similarly as above in section II(A), by viewing the disclosures of Katkoori and Shau, one can not jump to the conclusion of obviousness without impermissible hindsight

Neither Katkoori, Shau, nor the combination of the two, teach, disclose or suggest the limitations contained in Applicant's amended claims 10 and 24, as listed above. Since neither Katkoori, Shau, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claims 10 and 24, as listed above, there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claims 10 and 24 are not obvious over Katkoori in view of Shau since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 10 and 24, namely claims 11 and 25, respectively, would also not be obvious over Katkoori in view of Shau for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 11 and 25 are respectfully requested.

C. It is asserted in the Office Action that Claims 15-16 and 27-28 are rejected in the Office Action under 35 U.S.C. § 103(a), as being unpatentable over Katkoori in view of Ditlow. Applicant respectfully disagrees.

Applicant's amended claim 10 contains the limitations of "...determining an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA; dividing the set of equations representing the PLA into equations representing the plurality of sub-PLAs ; merging outputs of the equations representing the plurality of sub-PLAs; determining a topological circuit representation of the equations representing the plurality of sub-PLAs; applying gating logic to the topological circuit representation of the plurality of sub-PLAs; and controlling power consumption in the topological representation of the plurality of sub-PLAs so only one of the plurality of sub-PLAs contributes to power consumption, wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA."

Applicant's amended claim 24 contains the limitations of "...determine an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA; divide the set of equations representing the PLA into equations representing the plurality of sub-PLAs ; merge outputs of the equations representing the plurality of sub-PLAs; determine a topological circuit representation of the equations representing the plurality of sub-PLAs; apply gating logic to the topological circuit representation of the plurality of sub-PLAs; and control power consumption in the topological circuit representation of the plurality of sub-PLAs so only one of the plurality of sub-PLAs contributes to power consumption, wherein an OR plane of the topological circuit representation of a first sub-PLA is one of interleaved and separated with an OR plane of the topological circuit representation of a second sub-PLA."

Katkoori is discussed above in section I regarding Applicant's amended claims 10 and 24. As asserted above, nowhere does Katkoori disclose, teach or suggest "determining an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA" or "determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each have an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA."

Ditlow discloses a PLA having a decoder attached at the input of the PLA to only power up a portion of the PLA to minimize power consumption. Ditlow does not teach, disclose or suggest dividing a PLA into sub-PLAs where each sub-PLA has an OR plane. Ditlow does not teach, disclose or suggest "determining an optimum splitting variable for dividing a set of equations representing a programmable logic array (PLA) into equations representing a plurality of sub-PLAs, each sub-PLA of said plurality of sub-PLAs having an OR plane, said splitting variable corresponding to a specific input, output and product in the set of equations representing the PLA" or "determine an optimum splitting variable for dividing a programmable logic array (PLA) into a first sub-PLA and a second sub-PLA, said first sub-PLA and said second sub-PLA each have an OR plane, said splitting variable corresponding to a specific input, output and product in a set of equations representing the PLA."

Moreover, similarly as above in section II(A), by viewing the disclosures of Katkoori and Ditlow, one can not jump to the conclusion of obviousness without impermissible hindsight

Neither Katkoori, Ditlow, nor the combination of the two, teach, disclose or suggest the limitations contained in Applicant's amended claims 10 and 24, as listed above. Since neither Katkoori, Ditlow, nor the combination of the two, teach, disclose or suggest all the limitations of Applicant's amended claims 10 and 24, as listed above,

there would not be any motivation to arrive at Applicant's claimed invention. Thus, Applicant's amended claims 10 and 24 are not obvious over Katkoori in view of Ditlow since a *prima facie* case of obviousness has not been met under MPEP §2142. Additionally, the claims that directly or indirectly depend from amended claims 10 and 24, namely claims 15-16, and 27-28, respectively, would also not be obvious over Katkoori in view of Ditlow for the same reason.

Accordingly, withdrawal of the 35 U.S.C. § 103(a) rejections for Claims 15-16 and 27-28 are respectfully requested.

CONCLUSION

In view of the foregoing, it is submitted that claims 1-3, 6-19, and 22-40 patentably define the subject invention over the cited references of record, and are in condition for allowance and such action is earnestly solicited at the earliest possible date. If the Examiner believes a telephone conference would be useful in moving the case forward, he is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: June 2, 2004

By: _____

Steven Laut, Reg. No. 47,736

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail with sufficient postage in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P. O. Box 1450, Alexandria, Virginia 22313-1450 on June 2, 2004.

Jean Sroboda